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Low Power Consumption NOC Based Reconfigurable Routers for Data Movement

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ABSTRACT
The use of a reconfigurable router is proposed in this paper, where the buffer slots are dynamically allocated for increasing router efficiency in NoC, even under rather different communication loads. Power consumption and power related issues have become a concern for most designs & as fundamental barriers for many others. Network-on-chip (NoC) architectures are more scalable, reliable on-chip communication infrastructure platform. Technique used is clock gating which is to reduce chip dynamic power. System on Chip (SoC) is network version which means that on chip transmission is done through packet based networks.

Keywords: Buffer, Latency, Network-On-Chip, Power Consumption, Reconfigurable Router.

INTRODUCTION
The high demand for performance in processor hindered by the power consumption which has lead computer architects to design multi-processor & multi-core single chip architectures. Network-on-Chip (NoC) [1] is most efficient and scalable answer for the on-chip communication as it guarantees scalable high-speed transmission with minimal wiring overhead and physical routing issues. NoCs are now being considered by many, as alternative to design scalable communication architecture for present and future prospective. NoC comprises of routers & network interfaces .One or More Cores Connected to a network interfaces. Mainly in NoCs, routing algorithms are used for determining the path of a packet from the source to the destination. Different types of algorithms are deterministic and adaptive [2]. Deterministic routing algorithms are simple so easy for implementation but they are not able to balance the load across the links in non-robust traffic. Basically, a packet-based NoC consists of routers, the network interface between the routers, processing unit & the interconnection network. Design and innovative researches in VLSI circuits includes tradeoff between areas, speed along with power. Different on chip router methodologies are carried out to reduce power which increases speed. For providing efficient router for NoC, many methods were introduced at Network Interface kernel part of the router which consists of buffer, control unit, routing unit and some queuing or scheduling unit. For reducing IP core power, IP level low power methods must be used. IP level clock gating is to reduce power level in IP core. NoC can be known by its topology and by the methods used for routing, flow control, switching, and arbitration and buffering. As network topology describes nodes & channels into a graph. Routing [8] tells how a packet chooses a path & flow control describes the allocation of channels and buffers to a packets as it moves along the path. Switching is the mechanism that filters data from an input channel & output channel, arbitration is responsible to schedule the use of channels and buffers by the packets. Buffering describes the method used to store packets.
For delivering a packet [7] to its destination is to find the destination network address and then to route the packet to the destination network by using different routing algorithms. This implies each network is uniquely defined or traceable. Following is the diagram of NOC topology.

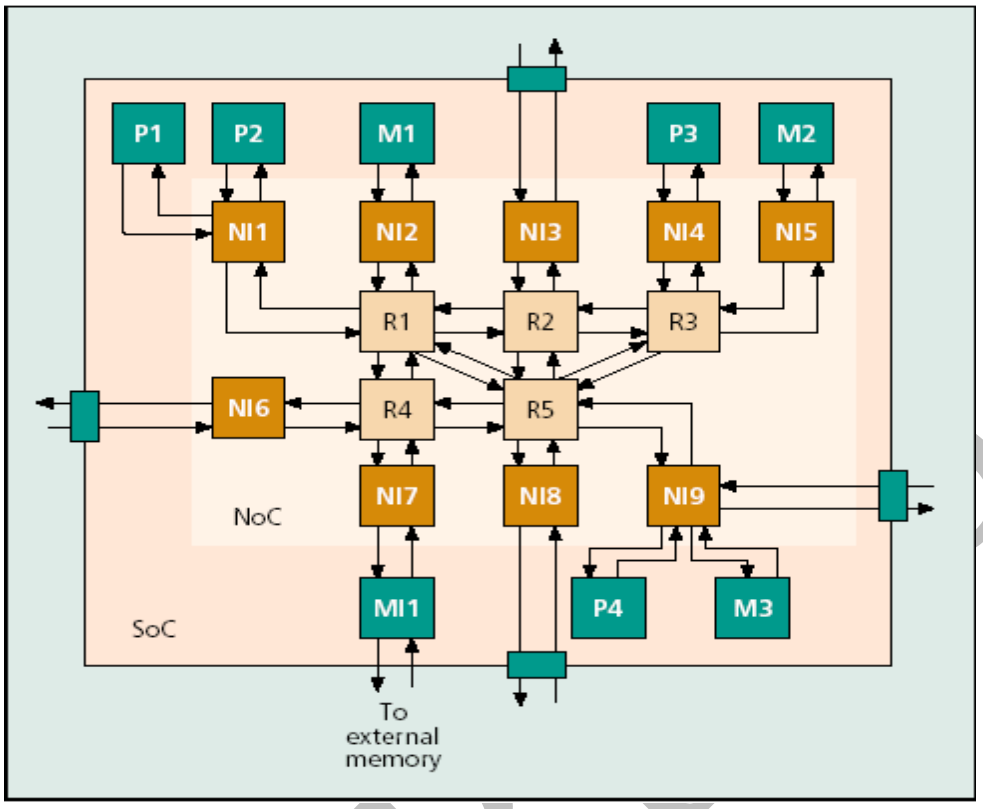


Fig1: NOC Topology

Many things in NoC can be varied from design to design, like depth of first-input–first-output (FIFO) buffers, router topology, switch and arbiter [5]. Results like throughput, latency and bandwidth are named as a modification in the NoC architecture.

Example of mixed communication behavior requirements is showed in the Fig. 2. In accordance with [3], there is a clear difference between traffic among cores in a SoC with out-of-order cores (OoCs) and in-order-cores (IoCs). However OoCs are larger& have worse power performance than IoCs.

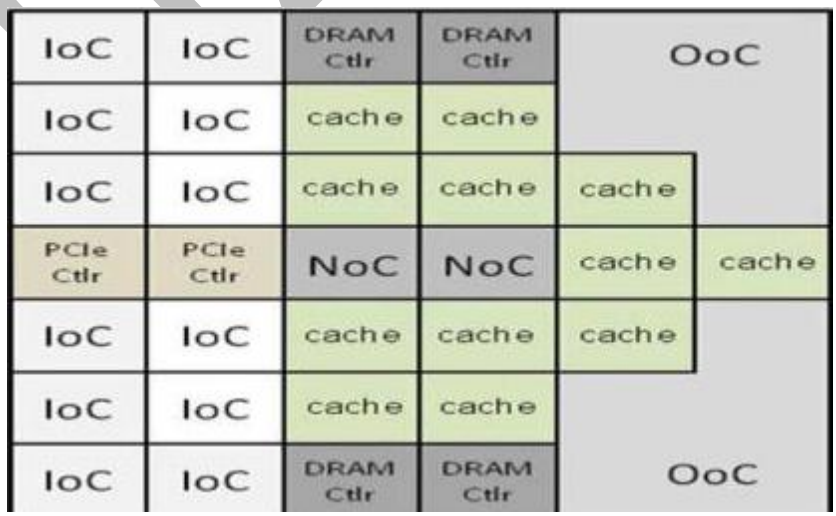


Fig 2: Example of different cores used in SoC

NoC components, such as crossbars, arbiters, buffers, and links, experiments realized that the buffers are the largest leakage power contender, dissipating approximately 64% of the whole power. The buffers were considered for leakage power optimization. The buffers' power consumption is also high, and it increases rapidly as the packet flow throughput increases. Providing the router with specific reconfiguration logic, allowing changes buffer utilization amount in each input channel, in conformity with the communication needs.

PROPOSED ROUTER ARCHTITECTURE

A. Original Router Architecture

SoCIN having regular 2-D-mesh topology having five bi-directional ports (Local, North, South, West, and East), each port with two unidirectional channels and each router connected to four neighbouring routers (North, South, West, and East). Such type architecture uses the wormhole switching approach and a deterministic source-based routing algorithm. Algorithm used for routing is XY-routing, which supports deadlock-free data transmission, and the flow control is based on the hand- shake protocol. Round robin arbiter is used at each output channel. At the input channel only buffering is present.

B. Reconfigurable Router Architecture

If NoC's router has a larger FIFO buffer, the throughput will be larger and the latency in the network smaller, since it will have fewer flits stagnant on the network. Nevertheless, there is a limit on the increase of the FIFO depth. Since each communication will have its peculiarities, sizing the FIFO for the worst case communication scenario will compromise not only the routing area, but power as well. If the router has a small FIFO depth, the latency will be larger, and quality of service (QoS) can be compromised. The proposed solution is to have a heterogeneous router, in which each channel can have a different buffer size

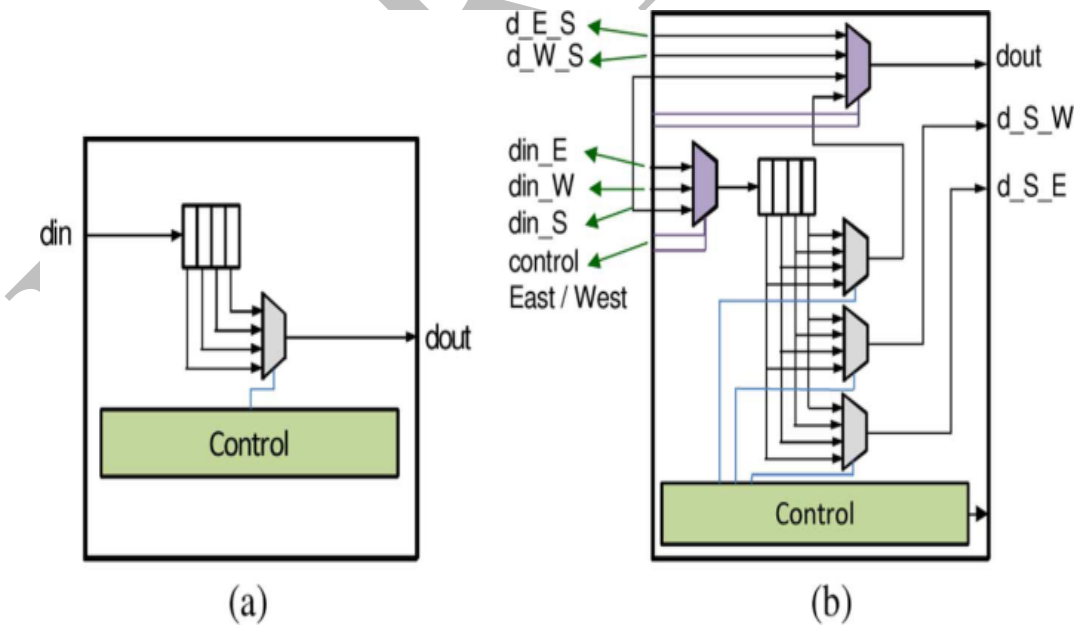


Fig 3 Input FIFO (a) original (b) proposed router.

Architecture is able to perform well because of the fact that not all buffers are used all the time. Here it is possible to reconfigure different buffer depths for each channel dynamically. A part or the whole of its buffer slots is given according to the requirements of the neighbouring buffers. For reducing costs, each channel may use only the available buffer slots of neighbour. Fig. 3 shows the original and proposed input FIFO. Comparing the two architectures, the new proposal uses more multiplexers to allow the reconfiguration process. Fig. 3(b) represents the South Channel for an example. Here it is possible to configure different buffer depths for the channels. In this

figure, each channel has five multiplexers, and two of these multiplexers are responsible to control the input and output of data. The size of the multiplexers that control the buffer slots increases according to the depth of the buffer. These multiplexers are controlled by the FSM of the FIFO. Possibility of the Local Channel is not used here, only the South, North, West, and East Channel of a router can make the use of their adjacent neighbour. Fig. 4 shows the channel of Fig. 3(b) organized to constitute the reconfigurable router. Each channel can receive three data inputs. Considering the South Channel as an example, having inputs: the own input (din _S), the right neighbour input (din_ E), and the left neighbour input (din _W). For example, assume using a router having buffer depth of four, & there is a router that needs to be configured accordingly South Channel whose buffer depth equals nine, Channel East having buffer depth equal to two, whereas West Channel with buffer depth equal to one remained North Channel with buffer depth equal to four. In this situation, the South Channel needs to borrow buffer slots from its neighbour. East Channel occupies two of its four slots, so it can lend two slots to its neighbour, and then also the South Channel still needs more three buffer slots. West Channel occupies only one slot, so the remaining three slots can be lent to the South Channel. When the South Channel has a flit stored in the East Channel, so flit must be sent to the output, so it is passed from the East Channel to the South Channel (d_E _S), and so the flit is directly sent to the output of the South Channel (dout _S) by multiplexers. Output seen from the south channel (dout_ S) and two more outputs (d _S _E and d_ S_ W) to send the flits stored in its channel but belonging to neighbour channels when an input channel is connected to an output channel, the flits are sent one at a time, and the pointers updation takes place as after each flit is sent.

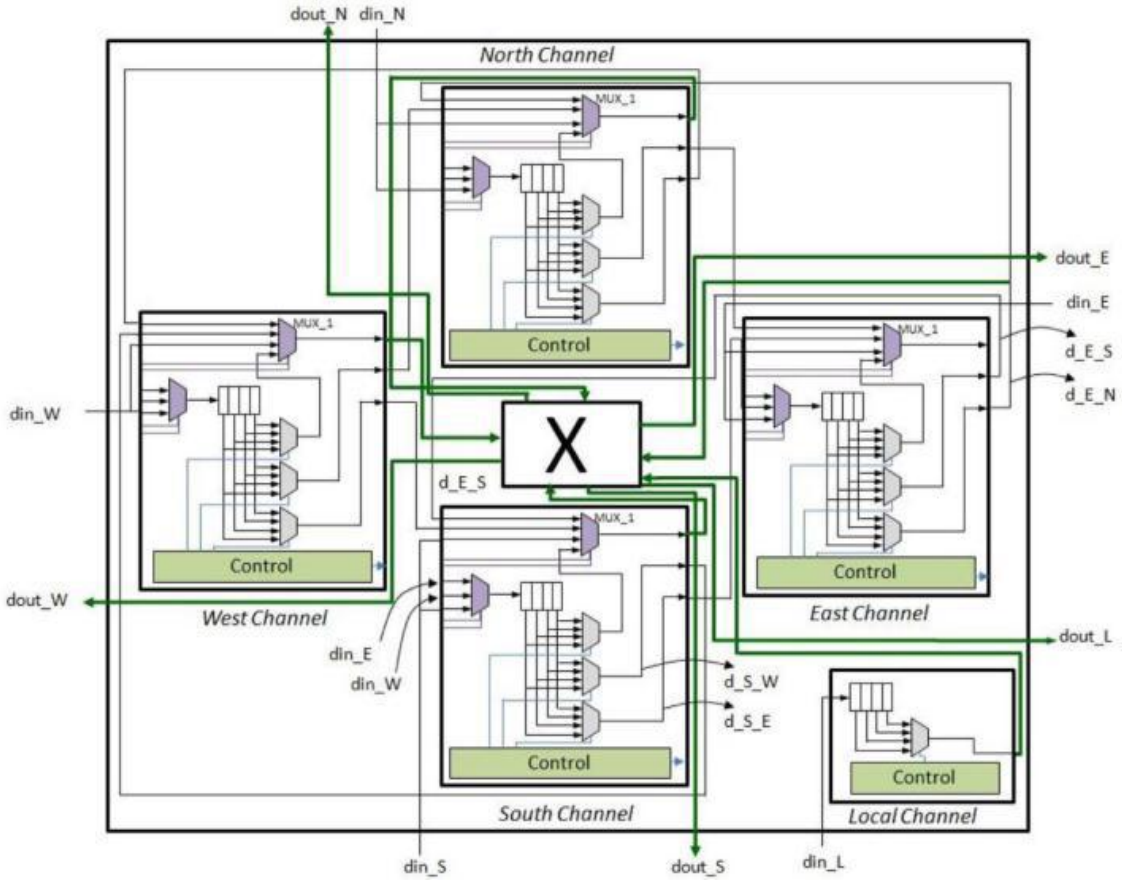


Fig.4.Proposed router architecture.

Reconfiguration [5] in a router is done according to a needed bandwidth in channel. Firstly, buffer depth for all channels is decided at design time, here we defined the buffer size equals four, as shown in Fig. 5(a).& then

traffic in each channel is verified and a control defines the buffer depth needed in each link to attend to this flow shown in Fig. 5(b).

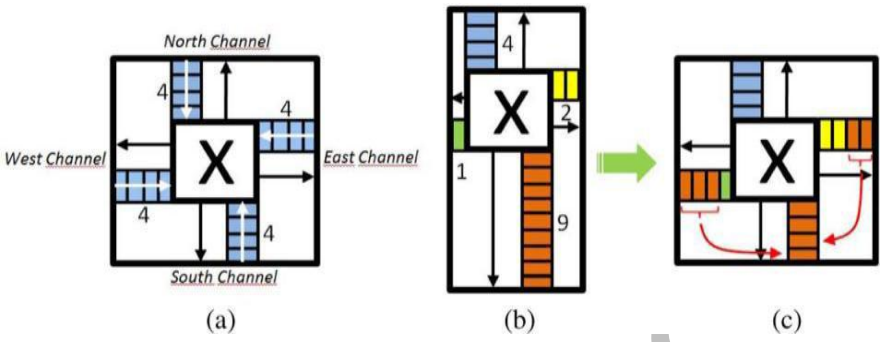


Fig.5 (a) Router designed with FIFO depth 4 (b) need of configuration of the router (c) Reconfiguration of the buffers to accordingly.

Reconfiguring channel according to the availability of buffers & if new depth is required, and then buffer depth is increased slot by slot, and change is done whenever a buffer slot is free. Whenever the application is changed, a different bandwidth is required among the channels. The reconfigurable router can change its depth in only few cycles, which means a very small performance overhead.

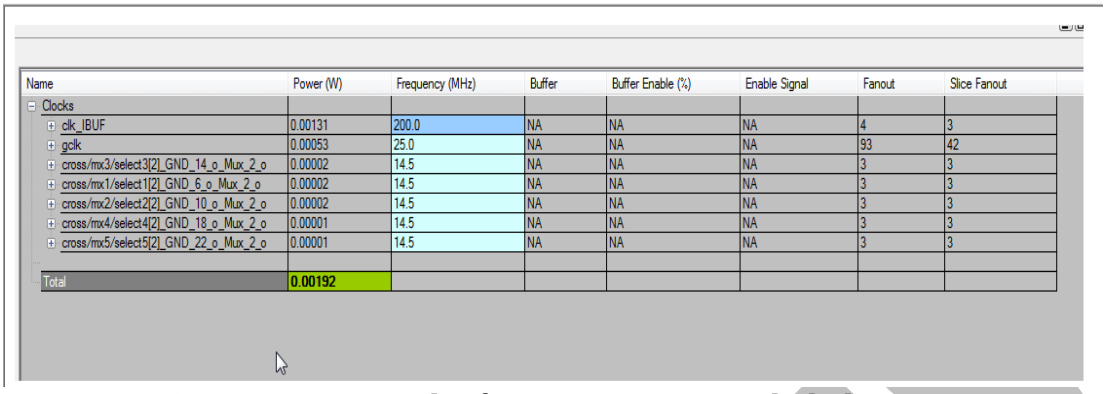
SIMULATION RESULTS

Router is described in Verilog HDL & Model Sim tool is used to simulate the code. We analyzed the average power consumption, & frequency results in Spartan FPGA kit on Xilinx tool. Largest power dissipation comes from the flip flops of the buffers in the router. By using the proposed reconfiguration, and by using extra multiplexers it became possible to reduce the total number of required flip-flops. One can still obtain power reduction because the multiplexers present less power consumption than flip-flops. A flip-flop dissipates power even when no data changes at its input, since the clock is always switching. So clock gating is useful technique. So power is analyzed at certain frequency with & without clock gating [4]. Data selector is another name of multiplexer. They are used in CCTV. As the link size increases, the amount of power savings increases which is allowed by the reconfigurable router. So we can say by seeing results that the proposed NoC router does not degrade the system performance, and can save power

Power Reduction using clock gating

Name	Power (W)	Frequency (MHz)	Buffer	Buffer Enable (%)	Enable Signal	Fanout	Slice Fanout
Clocks							
clk_BUFGP/IBUFG	0.00278	200.0	NA	NA	NA	93	39
cross/mx1/select1[2]_GND_4_o_Mux_2_o	0.00002	14.5	NA	NA	NA	3	3
cross/mx2/select2[2]_GND_8_o_Mux_2_o	0.00002	14.5	NA	NA	NA	3	3
cross/mx3/select3[2]_GND_12_o_Mux_2_o	0.00002	14.5	NA	NA	NA	3	3
cross/mx4/select4[2]_GND_16_o_Mux_2_o	0.00002	14.5	NA	NA	NA	3	3
cross/mx5/select5[2]_GND_20_o_Mux_2_o	0.00001	14.5	NA	NA	NA	3	3
Total	0.00286						

Fig6: power consumed at frequency 200 MHz without clock gating



Name	Power (W)	Frequency (MHz)	Buffer	Buffer Enable (%)	Enable Signal	Fanout	Slice Fanout
Clocks							
clk_IBUF	0.00131	200.0	NA	NA	NA	4	3
gclk	0.00053	25.0	NA	NA	NA	93	42
cross/mx3/select3[2]_GND_14_o_Mux_2_o	0.00002	14.5	NA	NA	NA	3	3
cross/mx1/select1[2]_GND_6_o_Mux_2_o	0.00002	14.5	NA	NA	NA	3	3
cross/mx2/select2[2]_GND_10_o_Mux_2_o	0.00002	14.5	NA	NA	NA	3	3
cross/mx4/select4[2]_GND_18_o_Mux_2_o	0.00001	14.5	NA	NA	NA	3	3
cross/mx5/select5[2]_GND_22_o_Mux_2_o	0.00001	14.5	NA	NA	NA	3	3
Total	0.00192						

Fig7: power consumed at frequency 200 MHz with clock gating

And so on different frequency with & without clock gating power consumed [6] by routers are calculated. The values are shown in tabular for easy understanding.

SNo.	FREQUENCY	POWER(without clock gating) in W	POWER(with clock gating) in W
1.	100 M Hz	0.00096W	0.00143W
2.	200 M Hz	0.00286W	0.00192W
3.	300 MHz	0.00429W	0.00288W

CONCLUSION

The availability of accurate, comprehensive power models are emerging key elements for low power design. The same performance obtained with the reconfigurable router the original architecture needs many more buffers. While new router, reached the same performance than the original architecture, obtained a reduction of approximately 25% of power consumption in the worst case. So obtaining low power increases the demands and also its working fields with no heavy monetary inputs as compared to original routers. However with the new architecture possible to recon figure the router according with the application, obtaining similar performances even when the application changes radically.

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